What is claimed :

1. A flash memory system comprising:

an array of flash memory cells;

four local bit lines positioned generally parallel with each other;

a first and a second global bit line;

a first multiplex circuit to selectively couple a first pair of the four local bit lines with the first global bit line, wherein the first pair of local bit lines are separated by one of the four local bit lines; and

a second multiplex circuit to selectively couple a second pair of the four local bit lines to the second global bit line.

2. The flash memory system of claim 1 wherein:

the first multiplex circuit comprises first and second select transistors, the first select transistor is coupled between a first local bit line of the four local bit lines and the first global bit line, the second select transistor is coupled between a third local bit line of the four local bit lines and the second global bit line; and

the second multiplex circuit comprises third and fourth select transistors, the third select transistor is coupled between a second local bit line of the four local bit lines and an the second global bit line, the fourth select transistor is coupled between a fourth local bit line of the four local bit lines and the second global bit line.

3. The flash memory system of claim 2 further comprising:

a first select line coupled to control gates of the first and second select transistors; and

a second select line coupled to control gates of the third and fourth select transistors.

4. The flash memory system of claim 1 wherein the array of flash memory cells is positioned between the first multiplex circuit and the second multiplex circuit.

5. The flash memory system of claim 1 wherein the flash memory cells are floating gate memory cells.

6. The flash memory system of claim 1 wherein the array of flash memory cells is arranged in rows and columns.

7. The flash memory system of claim 1 wherein the array of flash memory cells is positioned adjacent the first and second multiplex circuits.

8. The flash memory system of claim 1 wherein each of the flash memory cells is comprised of a floating gate capable of holding a charge.

9. The flash memory system of claim 8 wherein a presence or absence of the charge determines a state of the flash memory cell.

10. A flash memory system comprising:

an array of floating gate memory cells;

a plurality of local bit lines positioned generally parallel with each other;

a plurality of global bit lines such that there are twice as many local bit lines as global bit lines;

a first multiplex circuit to selectively couple a first pair of the plurality of local bit lines with a first global bit line of the plurality of global bit lines, wherein the first pair of local bit lines is separated by one of the plurality of local bit lines; and

a second multiplex circuit to selectively couple a second pair of the plurality of local bit lines to a second global bit line of the plurality of global bit lines.

11. The flash memory system of claim 10 wherein each global bit line of the plurality of global bit lines is selectively coupled to alternating local bit lines of the plurality of bit lines.

12. The flash memory system of claim 10 wherein the plurality of local bit lines is formed on a first metal level and the plurality of global bit lines is formed on a second metal level.

13. The flash memory system of claim 10 wherein the system is manufactured such that the plurality of local bit lines is on a different level than the plurality of global bit lines.

14. The flash memory system of claim 10 wherein the array of flash memory cells is floating gate memory cells arranged in rows and columns.

15. A flash memory system comprising:

an array of floating gate memory cells;

a plurality of local bit lines positioned generally parallel with each other;

a plurality of global bit lines such that there are twice as many local bit lines as global bit lines;

a first multiplex circuit to selectively couple a first set of the plurality of local bit lines with a first global bit line of the plurality of global bit lines, wherein the local bit lines of the first set are not adjacent local bit lines; and

a second multiplex circuit to selectively couple a second set of the plurality of local bit lines to a second global bit line of the plurality of global bit lines wherein the local bit lines of the second set are not adjacent local bit lines.

16. The flash memory system of claim 15 wherein the multiplex circuits comprise:

a plurality of select transistors coupled between an associated local bit line and an associated global bit line, each select transistor having a control gate.

17. The flash memory system of claim 16 and further including a plurality of select lines, each select line coupled to a control gate of a select transistor of the plurality of select transistors.

16. The flash memory system of claim 17 wherein the array of floating gate memory cells is located between the first multiplex circuit and the second multiplex circuit.

17. The flash memory system of claim 16 wherein the plurality of select transistors are located at opposite ends of the array of floating gate memory cells.

18. The flash memory system of claim 15 wherein the plurality of local bit lines are located on a different level than the plurality of global bit lines.

19. The flash memory system of claim 15 wherein at least one local bit line of the plurality of local bit lines is located above a drain diffusion region.

20. The flash memory system of claim 15 wherein the array of floating gate memory cells is arranged in rows and columns.